The University of Florida's next-generation cryogenic infrared focal plane array controller system

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ABSTRACT

The Infrared Instrumentation Group at the University of Florida has substantial experience building IR focal plane array (FPA) controllers and seamlessly integrating them into the instruments that it builds for 8-meter class observatories, including writing device drivers for UNIX-based computer systems. We report on a design study to investigate implementing an ASIC from Teledyne Imaging Systems (TIS) into our IR FPA controller while simultaneously replacing TIS's interface card with one that eliminates the requirement for a Windows-OS computer within the instrument's control system.

Keywords: FPA controllers, MCE-4, SIDCECAR ASIC, infrared
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1. INTRODUCTION

Modern low-noise infrared (IR) focal plane arrays (FPAs) only operate at cryogenic temperatures (7K to 70K) inside of a vacuum vessel. However, conventional control electronics for such IR FPAs are complicated, physically large, and reside outside of the cryogenic environment, as they only operate at room temperature. As a result, the analog video signals output from the IR FPA must travel a significant distance before they are digitized by the Analog-to-Digital Converters (ADCs), which can introduce significant degradation of the signals. Such large conventional IR FPA controllers will no longer be able to keep up with the demands required by modern astronomical instrument designs as the latter increase in complexity (e.g. multiple FPAs) and sensitivity requirements for lower noise performance.

Teledyne Imaging Sensors (TIS) has designed a programmable Application Specific Integrated Circuit (ASIC) called SIDECAR[1] ("System for Image Digitization, Enhancement, Control and Retrieval") which replicates all of the functionalities of a large conventional control system into a single integrated circuit (IC). Containing its own microprocessor, memory and ADCs, SIDECAR can be programmed to supply the drive voltages and clock signals required to run IR FPAs, and pre-amplify and digitize up to 36 channels of analog video output from the IR FPA. Most importantly, the ASIC operates at cryogenic temperatures[2] (T ~ 37 K) and as a result can be situated quite close to the IR FPA. Thus the IR FPA analog signals may be digitized before they have traveled even a fraction of the distance they would travel in a conventional control system. A further advantage of this ASIC is that it provides a completely digital interface to the outside environment, from which it will be controlled and the location where the IR FPA data will be sent.

TIS also has associated development kits, one for room temperature design work and one for cryogenic operation. The room temperature kit includes a SIDECAR ASIC, a circuit board for the SIDECAR ASIC and with test points, a JADE2 (JWST ASIC Drive Electronics) card, and an Integrated Development Environment (IDE) software package for learning how to operate the SIDECAR ASIC at the lowest levels. The JADE2 card is a digital interface between the ASIC and the external control computer. Commands to the ASIC and data from the ASIC are relayed by the JADE2 to an external control computer using a USB 2.0 port and running a third-party USB driver designed for the Windows XP operating

Ground-based and Airborne Instrumentation for Astronomy II, edited by Ian S. McLean, Mark M. Casali,
Proc. of SPIE Vol. 7014, 70146M, (2008) · 0277-786X/08/$18 · doi: 10.1117/12.788003

system. Thus, the TIS SIDECAR Development Kit provides instrument developers the starting point for integrating the SIDECAR ASIC into a complete modern cryogenic astronomical instrument.

However, this set of hardware and software is not a turn-key system suitable for immediate operation in a facility-class observatory instrument. Modern large observatories require flexible and speedy data acquisition from their instruments using very specific instrument configuration interfaces. These software configuration interfaces most commonly have been written for UNIX based hosts such as SunOS and varieties of Linux, while Windows-based systems are not in widespread use.

As the SIDECAR ASIC is a clear step forward for future infrared instruments, the Infrared Instrumentation Group at the University of Florida has obtained a room temperature SIDECAR ASIC Development Kit. We report here on the initial phases of a design study to investigate how to implement a SIDECAR ASIC into our IR FPA control system, which operates in a UNIX environment. We begin with a short description of the conventional control electronics used so far by our group, and then briefly describe some of the key details of the SIDECAR ASIC and of the development kit offered by TIS. We conclude with a description of the decision tree we will be evaluating in our study to integrate the SIDECAR ASIC into a complete, observatory-ready, cryogenic instrument.

2. CONVENTIONAL CONTROL ELECTRONICS IN AN OBSERVATORY ENVIRONMENT

The University of Florida Infrared Instrumentation Lab is a leader in the development of near- and mid-infrared imaging cameras and spectrometers for the world's largest astronomical telescopes. For example, we are presently building two major facility instruments: FLAMINGOS-2[3] (PI S.S. Eikenberry), a US$5.5M near-IR multi-object spectrometer and imager for Gemini Observatory, and Canari-Cam[4] (PI C. Telesco), a US$3.2M mid-IR imager, spectrometer, and polarimeter for the Gran Telescopio Canarias (GTC).

2.1 A brief description of MCE-4, a conventional FPA control system presently used by FLAMINGOS-2

Our present technology for controlling and reading out IR FPAs, called MCE-4, is a large conventional control system. Designed more than 10 years ago when it was state-of-the-art, the analog to digital (A/D) conversion in MCE-4 happens a large distance away (~ 4 m) from the FPA. A 4-U high power supply and an 8-U high VME enclosure (called MCE-4) with custom backplane are housed in a 19" rack thermal enclosure. The VME enclosure (panel (a) in Figure 1) contains a CPU card, a Pattern Generator Board (PGB), 16 ADC channels on 4 VME cards and a 16 channel Differential Amplifier Card, and an 'Upper Fiber' Board. Reference clock patterns and Digital-to-Analog (DAC) control signals generated by the PGB are input into the Bias-Clock board, which generates the final FPA biases and clocks for the IR FPA. The Bias-Clock board and the 32-channel preamp board are mounted on the dewar vacuum jacket together in a compartmentalized enclosure (panel (b) in Figure 1). The 32 analog output signals from the HAWAII-II FPA in FLAMINGOS-2 travel approximately 60 cm to exit the vacuum jacket and reach the preamplifier where they are multiplexed down to 16 output channels. They are filtered and amplified with a net gain of ~ 10.5; the signals travel ~ 3 m back to MCE-4 to the Differential Amplifier Card. The net gain of the analog signal, before reaching the ADCs, from the Preamp Card plus the Differential Amplifier Card is 5.3. The four A/D cards contain sufficient 32-bit memory to store two full HAWAII-II (2048^2 pixels) data frames, and the MCE-4 system can perform standard correlated-double-sampling (CDS) or correlated-multiple-sampling (CMS). In standard science data acquisition mode, the difference image from the correlated sampled images is output from a custom fiber converter card from EDT (www.edt.com) residing on the Upper Fiber Board and sent to an EDT PCI-bus fiber frame grabber card located ~ 4 m away in a UNIX host computer.

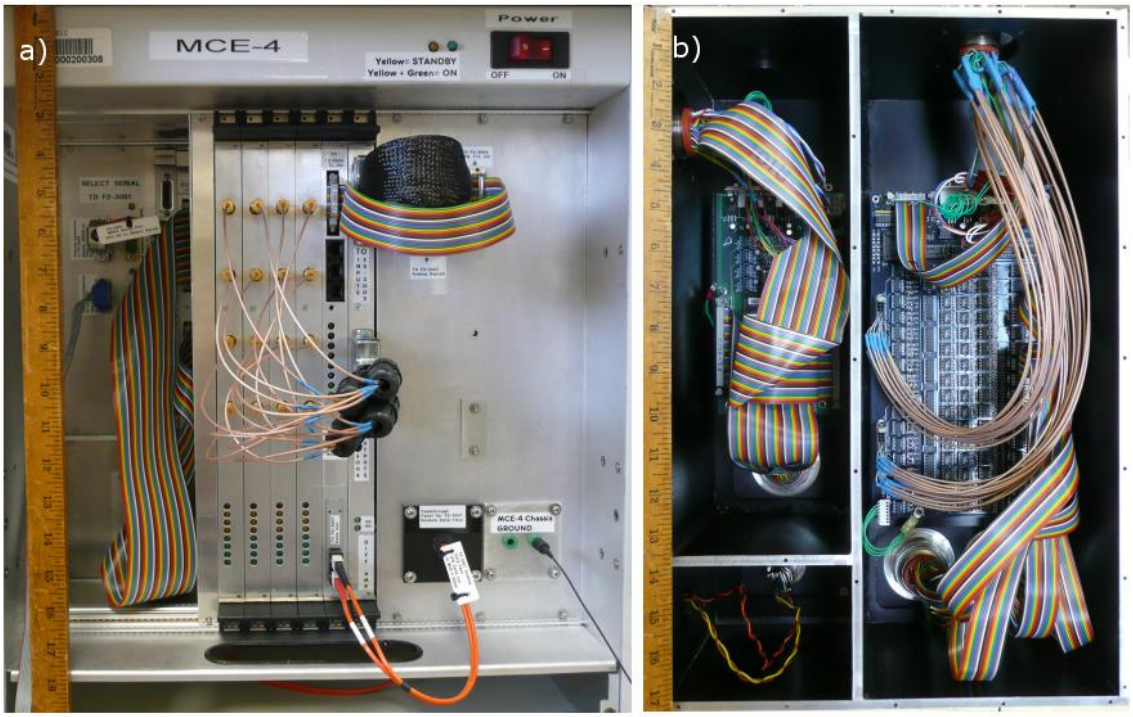

Figure 1 The FLAMINGOS-2 FPA controller system is a conventional room-temperature system. The 8-U VME MCE-4 is shown on the left in panel (a). The sixteen analog signals leads (tan) leaving the Differential Amplifier and entering the four ADC boards are visible. The Bias-Clock and Preamp boards are shown on the right in panel (b). These two boards are shielded from one another within the same metal enclosure that is mounted onto the Camera dewar vacuum jacket, close to the internal location of the science array.

Not including the separate bias and preamp boards, which are mounted on the dewar, this conventional control electronics system has several drawbacks. (1) It is large: the Gemini-standard thermal enclosure containing MCE-4 and its power supply is 24" wide × 31.25" deep × 51.25" high in size. (2) It is heavy: the populated thermal enclosure weighs 385 lb. (3) The power requirement for MCE-4 is high: since MCE-4 contains older high power memory and requires a large power supply the entire thermal enclosure dissipates ~ 260 W of power. Clearly, replacing this hardware with a SIDECAR ASIC could significantly reduce the size, weight and power requirements for the FPA control electronics.

2.2 The systems relationship of MCE-4 to FLAMINGOS-2 and the Gemini Observatory environment

The Gemini Observatory environment places a set of complicated requirements on the functional interfaces between each science instrument and the observatory. At the highest level, the Observatory Control System (OCS) sends instrument and observation configuration commands to the EPICS (www.aps.anl.gov/epics/) database Instrument Sequencer. For non-detector related configurations, these commands might include placing filters and grisms into the optical path inside of the instrument's dewar. Detector-related commands for a near-IR FPA might include changing the detector bias, setting the exposure time, and setting the number of multiple reads to perform during the integration. Finally, when ready, the OCS will instruct the Instrument Sequencer to command the detector controller to begin the integration.

As described in the previous section, FLAMINGOS-2's detector controller MCE-4 and its associated power supply reside in a single thermal enclosure. A separate thermal enclosure houses a UNIX host computer which runs the portable EPICS Instrument Sequencer and a suite of UNIX software agents; this separate thermal enclosure also contains electronics for controlling instrument mechanisms (*e.g.* filter and grism wheels) and monitoring dewar temperatures and pressures.

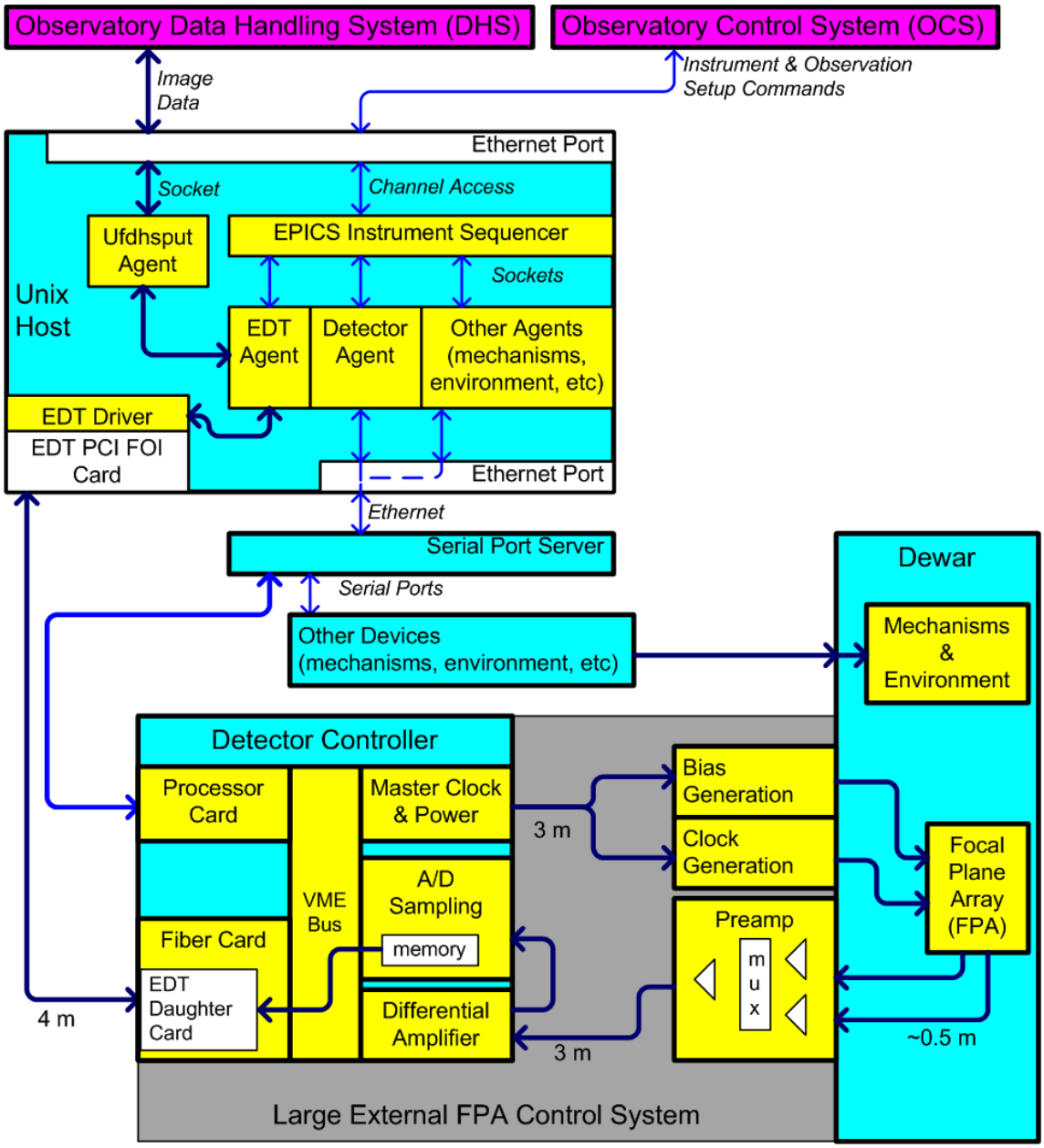

Figure 2. The FLAMINGOS-2 FPA controller system is a conventional room-temperature system designed to operate in the Gemini observatory environment, which places a set of complicated yet powerful requirements upon the instrument's functionality. The various subsystems of MCE-4 described in §2.1 are schematically indicated below the Detector Controller label in the figure. Section 2.2 describes relationship of MCE-4 to the UNIX host computer and the observatory environment.

The relationships between the UNIX host, the software agents, and the FLAMINGOS-2 MCE-4 detector control system are illustrated in Figure 2. OCS instrument configuration and observation commands (*e.g.* "start integrating") sent to the Instrument Sequencer are then relayed to the detector controller. Science data output from the detector controller are sent via fiber to the EDT frame grabber card on the UNIX host; these data are then queued-up by the UFDHSPUT agent before they are sent to the observatory Data Handling System (DHS) through another fiber. The image data are sent to the DHS in binary format, padded appropriately for FITS format; the DHS then concatenates the binary file with the relevant FITS header records for the observation to construct a FITS image file, and it handles all of the file naming. Thus, the instrument control system for FLAMINGOS-2 and the Observatory Control system require additional

hardware and computing resources to manipulate the data output from the MC-4 FPA controller, for every single exposure.

3. SIDECAR & THE DEVELOPMENT KIT

The next sections briefly summarize the key functional details of the SIDECAR ASIC that we will have to consider in our design study.

3.1 SIDECAR Functional Elements

In Figure 3 we illustrate the key elements of the SIDECAR ASIC (based on Loose, et al. 2003 and TIS's development kit brochure, available at www.teledyne-si.com/imaging/sidecar.html) and how they functionally relate to the operation of an IR FPA. SIDECAR requires only a few input signals from the outside world—a stable master reference clock is key, and it clearly also needs clean analog and digital power sources. All data input or output are relayed through a digital I/O interface using a custom protocol. Configuration programs input into SIDECAR's program memory are run by the microcontroller to produce clocks and digitally controlled analog signals to be output to the IR FPA; up to 32 clocks may be generated, as well as up to 20 analog voltages. The ASIC can address up to 36 analog inputs (i.e., outputs from the IR FPA), first amplifying and filtering the signals at a range of settings before sampling them with either 12-bit or 16-bit ADCs. Thirty-six array processor blocks allow the microprocessor to perform mathematical operations on the data before storing it in the main data memory. The main data memory is 36 kwords in size, at 24 bits/word.

TIS designed the SIDECAR ASIC to have the flexibility to operate a wide number of FPAs, as well as multiple arrays at a time. In Figure 3 we indicate that it can operate a HAWAII-2RG FPA. This FPA has 32 analog outputs for reading out the entire FPA, but it also includes an extra output for an on-chip guide window. In this mode a user-defined sub-region of the FPA may be read out at a higher rate than the rest of the FPA. The SIDECAR ASIC has sufficient microprocessor power, data memory, and speed to fully support this guide window mode.

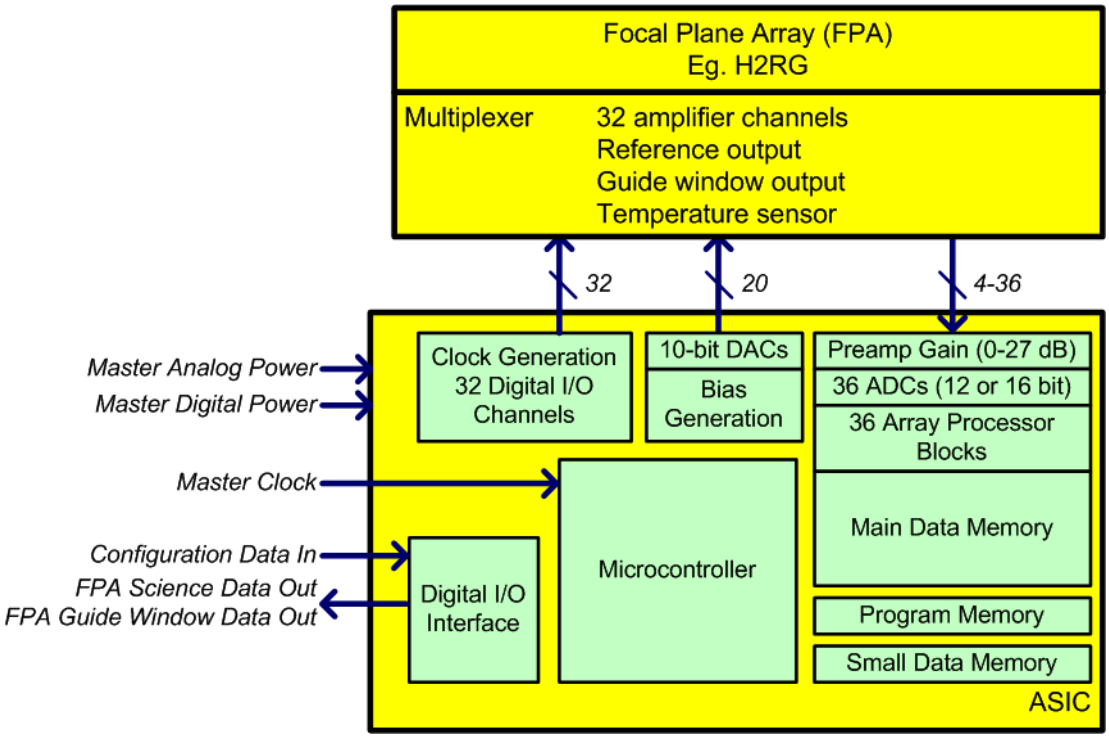

Figure 3. The block functional elements of the SIDECAR ASIC (adapted from Loose, et al 2003) are illustrated. All of the functional requirements to operate a HAWAII-2RG array are present. SIDECAR requires a minimum number of signal and power inputs, shown on the left, such as power and a reference clock. Configuration data in and science data out are transmitted through the same serial interface.

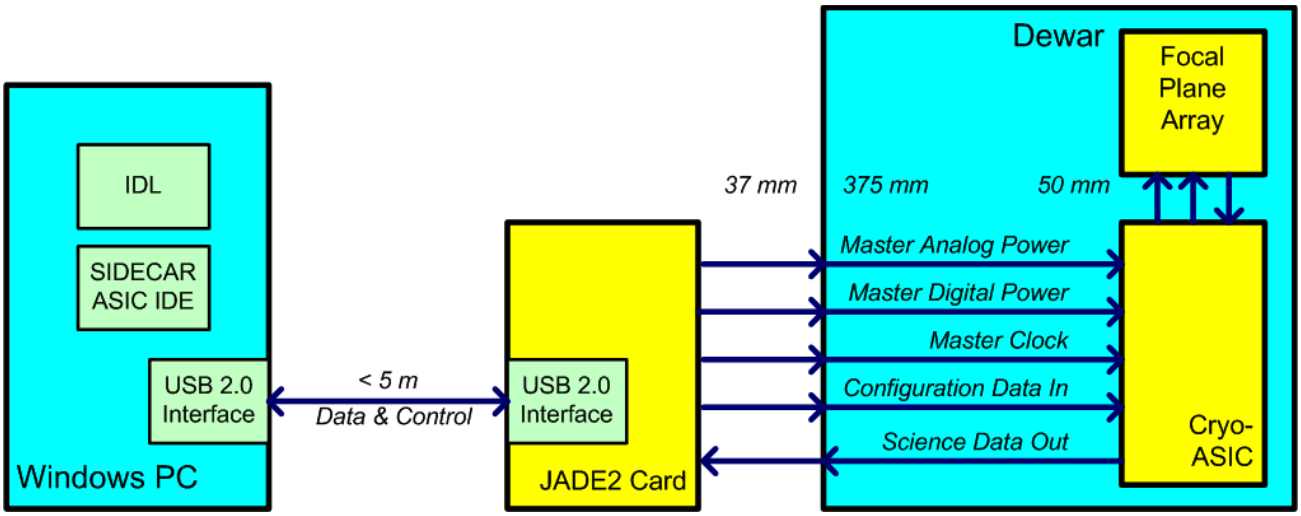

Figure 4. The TIS room temperature and cryogenic temperature kits include a custom JADE2 interface card which can be controlled by an IDE running on a Windows PC. The JADE2 card produces all of the required input signals for the ASIC described in §3.1 and in Figure 3. Data and control signals between the JADE2 card and the Windows PC are transmitted over a USB 2.0 cable.

3.2 SIDECAR plus JADE2 development kit

The two development kits offered by TIS include a JADE2 card in order to interface the SIDECAR ASIC to a PC; see Figure 4. The JADE2 card outputs all the required digital and analog power and the master clock signal required by the SIDECAR ASIC; it also transmits the data into and out of the ASIC using the custom protocol. In turn, the JADE2 card has a USB 2.0 interface for its connection to a host computer. The development kit includes an IDE which runs on Windows XP and a third-party USB driver to allow the IDE to communicate with the JADE2. In the IDE all of the low-level details of the ASIC are visible, while the translations of the commands into the ASIC's actual custom protocol are hidden.

4. WAYS TO INCORPORATE A SIDECAR ASIC INTO AN INSTRUMENT

The SIDECAR ASIC was introduced to the astronomical community at least 5 years ago[1], and NASA's Goddard Space Flight Center is presently involved in laboratory studies of the ASIC's technical readiness level (TRL) for space based applications; it is a key component of the detector controller for the NIRSpec instrument on JWST[5]. There is also significant interest in utilizing the SIDECAR ASIC in ground-based instruments for major observatories, but we are not aware that any have yet been deployed. For example the UCLA and Caltech instrumentation teams building MOSFIRE[6] for Keck Observatory have chosen the SIDECAR ASIC for its detector controller, but MOSFIRE is not scheduled for delivery until late 2009 to early 2010.

We see at least three options for incorporating a SIDECAR ASIC into an observatory-ready instrument design:

1. Use only the SIDECAR ASIC, and design our own custom interface card;
2. Use the SIDECAR ASIC, the JADE2 interface card, but eliminate the Windows PC;
3. Use the SIDECAR ASIC and the JADE2 interface card, and a Windows PC.

4.1 Option 1: A system without a JADE2 card or a Windows PC

Loose et al. (2003) indicate that it should be possible to build a simple interface to the ASIC utilizing one of the newer generation of FPGAs (Field Programmable Gate Arrays), with all of the required speed and infrastructure (such as a CMOS or LVDS digital interface). Our current conventional system, MCE-4, utilizes three XILINX XC4013E chips per A/D card. These chips are no longer available, and have not been since approximately 2003. One risk to designing our own card, if it also uses one or more FPGAs, is that the chosen FPGA might soon become obsolete. Thus it probably is best to attempt a design that is not so complicated that it cannot be easily updated and utilize newer chips.

The JADE2 card uses a USB 2.0 interface for both the input of configuration commands to execute the next integration and to transfer the science data out of the ASIC. In contrast, in our MCE-4 system the input of configuration commands and the output of science data are split to two different interfaces. Configuration commands to setup and execute the next integration are input into a simple serial interface which also has two RS232-to-Fiber converter boxes on either end, to further isolate the detector control system. These configuration commands are sent to MCE-4 from the detector agent operating on the UNIX host. Similarly, science data are sent over a fiber from the MCE-4 Upper Fiber Board using a custom EDT fiber converter card to the EDT frame grabber card in the instrument's UNIX host. Any design with a custom card will need to consider utilizing a fiber converter card and fiber frame grabber (EDT or from some other vendor), as they eliminate additional return paths for ground loops and noise introduction.

Our MCE-4 system also contains enough memory to store two entire HAWAII-2 frames in order to manipulate the data for CDS and CMS readout modes. In CDS mode it stores the two image reads taken at the start and end of the integration and the output image is the difference of the two images. CMS mode is similar in that it sums the set of individual sample frames at the beginning of the integration and the set of individual sample frames taken at the end of the integration into two images and then outputs the difference of the two summed images. Another decision point is whether or not a custom card should have any of its own memory. Including enough memory to store two full HAWAII-II frames increases the complexity of the design for the interface card when considering this option. It possibly significantly increases the complexity at the coding and hardware levels in order properly address all of this memory. In comparison, the JADE2 card appears to just transfer received data to the PC without performing any intermediate storage or manipulation. Not having any memory in the custom card would lead to more software effort in the UNIX platform, but may reduce the overall system complexity.

4.2 Option 2: A system with a JADE2 card but no Windows PC

TIS provides a third-party USB 2.0 driver to allow the IDE running on the Windows XP host to communicate with the ASIC through the JADE2 card. Retaining the JADE2 card, but eliminating the Windows PC would require a USB 2.0 driver that worked on the UNIX host and operating system used for the rest of the instrument. In the case of FLAMINGOS-2, this host is a Sun V210 running Solaris 10. Having to write a custom USB driver for a particular operating system may have its own risks, as compared to the risk of selecting a FPGA described in the previous option. Several considerations when using the JADE2 card are 1) it no longer has the electrical isolation provided by the two fibers in the present MCE-4 system, since the JADE2 card would be wired to the computer using a USB 2.0 cable, and 2) the maximum cable length for a USB 2.0 cable is 5 m.

The data handling software in such a system probably becomes more complicated. In FLAMINGOS-2 there are separate agents for commands to MCE-4 and acquisition of data from MCE-4, which occur on different hardware ports. In a JADE2 system, both output and input would be from the same port, which may require the agents to be combined.

Another complication arises in "guide-box mode" of HAWAII-2RG arrays. This mode allows a user-defined sub region of the FPA to be read at a faster rate than the entire array, such that a point source's centroid could be used for tip-tilt guiding corrections. This guide data will also be entering on the same port and will need to be sent to the A&G system.

4.3 Option 3: A system with a JADE2 card and a Windows PC

The MOSFIRE detailed design review (DDR) documentation is publicly available on their website (www.astro.ucla.edu/~irlab/mosfire/), and it provides some critical examples of the decisions that need to be made to operate the ASIC in this configuration. They will use a Windows PC to interface to the JADE2 card and a separate Solaris computer to run their custom detector server software (i.e. the Windows PC will be hidden to the end user).

The TIS development kit comes with Microsoft .NET 2.0, a COM DLL, and a third-party USB 2.0 driver so that the kit's IDE can transparently interact with the ASIC. The MOSFIRE DDR document indicates that they are considering using Java Remote Method Invocation (RMI) to allow their detector server to call Java code on the Windows PC (across the network). However, their document indicates that they also had to find other third-party software for the Windows PC to 'bridge' from JAVA to COM, and that there might be some numeric issues with Java's lack of support for unsigned data types. Retaining the JADE2 card simplified the hardware requirements for the system, but appears to have substantially complicated the software, as it is now distributed across two different types of operating systems. We plan to contact the MOSFIRE team to inquire if they have found their solution to be effective and lower risk.

Finally, the MOSFIRE document indicates that the JADE2 card is best run off of a separate power supply. The JADE2 card provides all of the power and master clock required by the ASIC and an HAWAII-2RG array, but without at

separate power supply for the JADE2 card, it would have to source all of its power over the USB 2.0 cable from the potentially electrically noisy power on the Windows PC.

5. CONCLUDING THOUGHTS

Each of the three solutions to integrating a SIDECAR ASIC into our detector control system has distinctly different advantages and disadvantages. Whichever one is chosen, it needs to retain all of the functionality provided by the ASIC. For example, the SIDECAR ASIC can fully support guide mode of operation of a HAWAII-2RG FPA. Our solution needs to

- Allow speedy changes between CDS and CMS modes of readout with and without a guide box;
- Allow definition into the ASIC of the guide box location and size;
- Allow high-speed output of the guide box data during a long integration on the rest of the array.

One of our options replaces the JADE2 card with own custom interface card to the SIDECAR ASIC, while the other two options retain the JADE2 interface card. In either case, guide box data probably need to be sent to the observatory Acquisition & Guiding (A&G) system, and not to the same location as the science data (e.g., the DHS at Gemini). We need to know the range of readout bit rates for the guide mode. If the guide data are sent to a computer host on the instrument prior to going to the A&G system, does this host need to have a real-time operating system? A non-real-time operating system might periodically interrupt the guide data stream in order to take care of some other process or house-keeping activities, which could affect the guide performance.

Similarly, the SIDECAR ASIC can only hold 36K pixels in memory, which means that data from a HAWAII-2RG FPA will be output by the ASIC in chunks of this size (possibly continuously or in packets). We need to ensure that our method to interface with the ASIC can match the data rate from the ASIC. Also, SIDECAR's data memory limitations imply that the destination computer will have to perform the final summation or differencing of each read set taken in CDS or CMS read modes.

Finally, TIS provides example SIDECAR microcode for reading out an HAWAII-2RG array with the development kit; they will also provide guide mode code, for an additional fee. Several important considerations for the system without the JADE2 card (and possibly even for the ones with the JADE2 card):

- If TIS only provides the high-level source-code (i.e. in human-readable format) how do we assemble it into the correct binary format? Can the development kit IDE be used to assemble and save it in this format? Or do we have to write our own assembler?
- Once we have the binary file, do we download it into the ASIC every time from the host computer? If more than one operational program frequently needs to be run, and hence downloaded into the ASIC every time, is it better to store it in hardware (e.g. in a EPROM) within the detector controller system than to transmit it from the host computer?

TIS's SIDECAR ASIC is an exciting development for infrared instrument designers. New instruments will be able to have a much more compact FPA control system which is more flexible in the manner, type and number of FPAs it can operate. Its ability to operate in a cryogenic environment allows it to digitize the FPA analog output signal very quickly, resulting in higher quality data.

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